II. The Drawings Satisfy All Formal Requirements

The Office Action objects to the drawings based on informalities. Specifically, the Office Action asserts that reference number 34 is not mentioned in the specification. Applicant respectfully submits that item 34 in Fig. 1 is described as a "jig" in the specification at page 20, line 23. No drawing corrections are needed. Withdrawal of the objection to the drawings is respectfully requested.

III. Claims 2-8 Satisfy the Requirements under 35 U.S.C. §112, second paragraph

The Office Action rejects claims 2-8 under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 2 and 3 have been amended to obviate this rejection. Withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

IV. Claims 1-5, 7 and 8 Define Patentable Subject Matter

The Office Action rejects claims 1-5, 7 and 8 under 35 U.S.C. §102(b) over U.S. Patent 5,239,448 to Perkins *et al.* (Perkins). This rejection is respectfully traversed.

Perkins does not teach or suggest an interconnect substrate including a first substrate on which a first interconnect pattern is formed, and a second substrate on which a second interconnect pattern is formed, wherein the first and second substrates are disposed so as to overlap each other but so as not to be in contact with each other, at least one of the first interconnect pattern and the second interconnect pattern has a mounting region for an electronic chip, and the first interconnect pattern and the second interconnect pattern are electrically connected, as recited in claim 1.

Instead, Perkins discloses a method of fabricating a multichip module (MCM) in which a flexible substrate 2 based on a stiffener 40 and overlayed by circuit layers 4, 6 and a first dielectric layer 8. Perkins further teaches a circuit layer 12 and the second dielectric layer 14 attached to the first dielectric layer 8. The first dielectric layer 8 is penetrated by

vias 10 filled with conductive material 11 that connect the circuit layers 6 and 12 together. See col. 4, lines 3-21, 33-50, col. 6, lines 31-49, col. 7, lines 20-23 and Fig. 8 of Perkins.

There is no teaching or suggestion in Perkins for first and second substrates connected together by an adhesive, as recited in Applicant's claims. Rather, Perkins discloses forming the first dielectric layer 8 over the circuit layer 6 and the substrate 2, and forming the second dielectric layer 14 over the circuit layer 12 and the first dielectric layer 8 by conventional means, such as hot roll lamination. See col. 6, lines 19-21 of Perkins. By using an adhesive to connect first and second substrates, Applicant provides advantages over the applied reference in expanded methods of substrate fabrication. Additionally, Applicant enables material characteristics of the adhesive that can be tailored for applications not limited by the properties of the substrate composition.

A claim must be anticipated for a proper rejection under §102(a), (b) and (e). This requirement is satisfied "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." See MPEP §2131.

For at least these reasons, Applicant respectfully asserts that independent claim 1 is now patentable over the applied reference. The dependent claims are likewise patentable over the applied reference for at least the reasons discussed as well as for the additional features they recite. Consequently, all the claims are in condition for allowance. Thus, Applicant respectfully requests that the rejections under 35 U.S.C. §102 be withdrawn.

V. Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Gerhard W. Thielman
Registration No. 43,186

JAO:GWT/gwt

Attachment:
Appendix

Date: April 22, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claims:

1. (Amended) An interconnect substrate ~~wherein~~ comprising:

a first substrate on which a first interconnect pattern is formed; and

a second substrate on which a second interconnect pattern is formed, wherein the first and second substrates are disposed ~~in superimposition~~ so as to overlap each other but so as not to be in contact with each other;

at least one of the first interconnect pattern and the second interconnect pattern has a mounting region for an electronic chip; and

the first interconnect pattern and the second interconnect pattern are electrically connected.

2. (Amended) The interconnect substrate as defined in claim 1, wherein:

the second substrate is larger than the first substrate, and

~~the~~ a whole surface of the first substrate is adhered to the second substrate.

3. (Amended) The interconnect substrate as defined in claim 1, wherein:

the first interconnect pattern is formed on ~~one~~ a first surface of the first substrate;

the second interconnect pattern is formed on ~~one~~ a second surface of the second substrate; and

a third surface of the first substrate opposite to the first surface ~~on which the first interconnect pattern is formed~~ and the second surface of the second substrate ~~on which the second interconnect pattern is formed~~ are disposed to oppose each other.

Claims 40 and 41 are added.